Fast Ultra High-PSRR, Low-Noise, Low-Dropout, 600mA Micropower CMOS Linear Regulator

General Description

The EMP8966 low-dropout (LDO) CMOS linear regulators, feature ultra-high power supply rejection ratio (75dB at 1kHz), low output voltage noise (30μV), low dropout voltage (270mV), low quiescent current (110μA), and fast transient response. It guarantees delivery of 600mA output current, and supports adjustable (1.2V to 5.0V) output voltage versions.

The EMP8966 is ideal for battery-powered applications by virtue of its low quiescent current consumption and its 1nA shutdown mode of logical operation. The regulator provides fast turn-on and start-up time by using dedicated circuitry to pre-charge an optional external bypass capacitor. This bypass capacitor is used to reduce the output voltage noise without adversely affecting the load transient response. The high power supply rejection ratio of the EMP8966 holds well for low input voltages typically encountered in battery- operated systems. The regulator is stable with small ceramic capacitive loads (2.2μF typical).

Additional features include regulation fault detection, bandgap voltage reference, constant current limiting and thermal overload protection. Available in miniature 5-pin SOT-23-5,SOT-23-6 package options are offered to provide additional flexibility for different applications.

EMP products is RoHS compliant.

Features

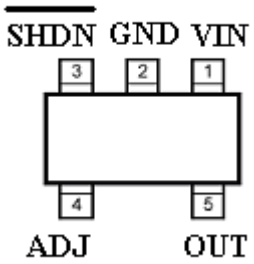
- Miniature SOT-23-5 and SOT-23-6 packages
- 600mA guaranteed output current
- 75dB typical PSRR at 1kHz
- 30μV RMS output voltage noise (10Hz to 100kHz)
- 270mV typical dropout at 600mA
- 110μA typical quiescent current
- 1nA typical shutdown mode
- Fast line and load transient response
- 80μs typical fast turn-on time
- 2.5V to 5.5V input range
- Stable with small ceramic output capacitors
- Over temperature and over current protection
- ±2% output voltage tolerance

Applications

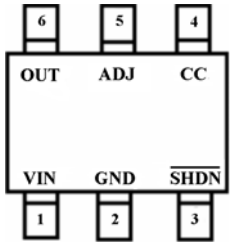
- Wireless handsets
- PCMCIA cards
- DSP core power
- Hand-held instruments
- Battery-powered systems
- Portable information appliances

Connection Diagrams

SOT-23-5(Top View)



SOT-23-6(Top View)



Order information

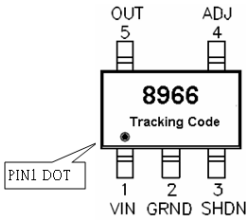
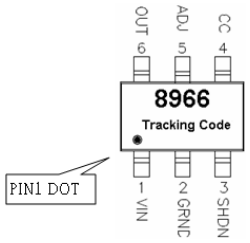
EMP8966-XXVF05GRR/NRR

XX	Operation Code
VF05	SOT-23-5 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

EMP8966-XXVC06GRR/NRR

XX	Operation Code
VC06	SOT-23-6 Package
GRR	RoHS (Pb Free)
	Rating: -40 to 85°C
	Package in Tape & Reel
NRR	RoHS & Halogen free (By Request)
	Rating: -40 to 85°C
	Package in Tape & Reel

Order, Mark & Packing Information

No. of PIN	Adj	EN	CC	Package	Marking	Vout Code (XX)	Vout	Product ID
5	Y	Y	N	SOT-23-5		00	Adj	EMP8966-00VF05GRR
6	Y	Y	Y	SOT-23-6		00	Adj	EMP8966-00VC06GRR

Old Marking: please see the notice(Page 18)

Package & Packing

SOT-23-5	3K units Tape & Reel
SOT-23-6	3K units Tape & Reel

Typical Application

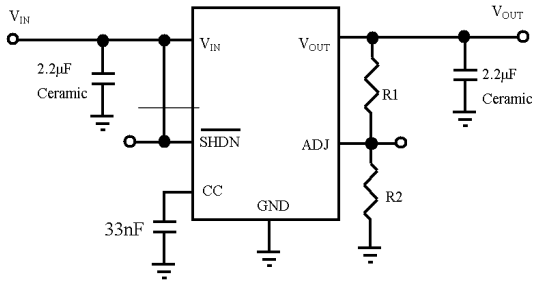


Fig. 1. EMP8966. Adjustable output version. Please refer to Application Information section for R1/R2 calculation.

Pin Functions

Name	SOT-23-5	SOT-23-6	Function
VOUT	5	6	**Output Voltage Feedback**.
VIN	1	1	**Supply Voltage Input**. Require a minimum input capacitor of close to 1μF to ensure stability and sufficient decoupling from the ground pin.
GND	2	2	**Ground Pin**.
ADJ	4	5	**Adjustable Negative Feedback Control**. Use external fixed resistors instead of trim pots to achieve the desired output voltage control.
CC		4	**Compensation Capacitor**. Connect an optimum 33nF noise bypass capacitor between the CC and the ground pins to reduce noise in VOUT.
$\overline{SHDN}$	3	3	**Shutdown Input.** Set the regulator into the disable mode by pulling the $\overline{SHDN}$ pin low. To keep the regulator on during normal operation, connect the $\overline{SHDN}$ pin to VIN. The $\overline{SHDN}$ pin must not exceed VIN under all operating conditions.

Absolute Maximum Ratings (Notes 1, 2)

VIN, VOUT, $V_{\overline{SHDN}}$, VSET, VCC, $V_{\overline{FAULT}}$	-0.3V to 6.0V
Power Dissipation	(Note 3)
Storage Temperature Range	-65°C to160°C
Junction Temperature (T_J)	150°C
Lead Temperature (10 sec.)	260°C
ESD Rating	
Human Body Model (Note 5)	2kV
MM	200V

Thermal Resistance (θ_{JA}) (Note 3)	
SOT-23-5	250°C/W
SOT-23-6	250°C/W

Operating Ratings (Note 1), (Note 2)

Temperature Range	-40°C to 85°C
Supply Voltage	2.5V to 5.5V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V_{IN} = V_{OUT} + 1V$ (Note 6), $V_{\overline{SHDN}} = V_{IN}$, $C_{IN} = C_{OUT} = 2.2\mu F$, $C_{CC} = 33nF$, $T_J = 25°C$. **Boldface** limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V_{IN}	Input Voltage		**2.5**		**5.5**	V
ΔV_{OTL}	Output Voltage Tolerance	100µA ≤ I_{OUT} ≤ 300mA $V_{OUT\ (NOM)}$ +0.5V ≤ VIN ≤ 5.5V (Note 6) ADJ = VOUT for the Adjust Versions	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
V_{OUT}	Output Adjust Range		**1.20**		**5.0**	V
I_{OUT}	Maximum Output Current	Average DC Current Rating	**600**			mA
I_{LIMIT}	Output Current Limit (SOT-23-5, SOT-23-6)		**600**	950		mA
I_Q	Supply Current	I_{OUT} = 0mA		110		µA
		I_{OUT} = 600mA		255		
	Shutdown Supply Current	V_{OUT} = 0V, $\overline{SHDN}$ = GND		0.001	1	
V_{DO}	Dropout Voltage (Note 4), (Note 6)	I_{OUT} = 50mA		22		mV
		I_{OUT} = 300mA		130		
		I_{OUT} = 600mA		270		
ΔV_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 7)	-0.1	0.02	0.1	%/V
	Load Regulation	100µA ≤ I_{OUT} ≤ 600mA		0.001		%/mA
e_n	Output Voltage Noise	I_{OUT} = 10mA, 10Hz ≤ f ≤ 100kHz		30		μV_{RMS}
$V_{\overline{SHDN}}$	$\overline{SHDN}$ Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 6)	**1.2**			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 6)			**0.4**	
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or VIN		0.1	100	nA
I_{ADJ}	ADJ Input Leakage	ADJ=1.3V,		0.1	3	nA
T_{SD}	Thermal Shutdown Temperature			165		℃

	Thermal Shutdown Hysteresis			30		
T_{ON}	Start-Up Time	C_{OUT} = 10µF, V_{OUT} at 90% of Final Value		80		µs

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
Note 2: All voltages are with respect to the potential at the ground pin.
Note 3: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the MSOP-8 package θ_{JA} = 223°C/W, T_J (MAX) = 150°C and using TA = 25°C, the maximum power dissipation is found to be 561mW. The derating factor (-1/θ_{JA}) = -4.5mW/°C, thus below 25°C the power dissipation figure can be increased by 4.5mW per degree, and similarity decreased by this factor for temperatures above 25°C.
Note 4: Typical Values represent the most likely parametric norm.
Note 5: Human body model: 1.5kΩ in series with 100pF.
Note 6: Condition does not apply to input voltages below 2.5V since this is the minimum input operating voltage.
Note 7: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 0.5V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.5V.

Functional Block Diagram

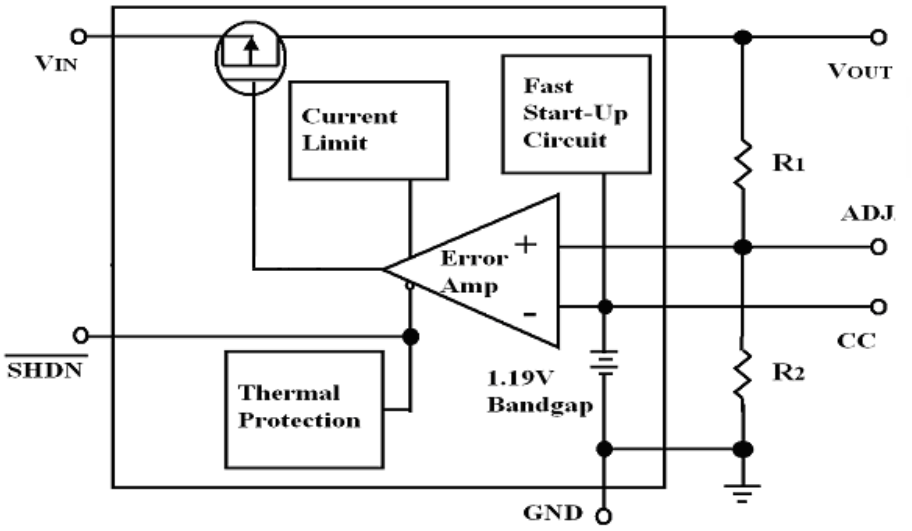
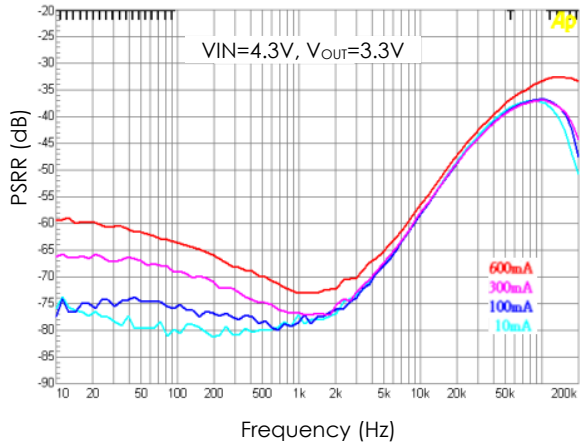


Fig.2. The EMP8966 Functional Block Diagram

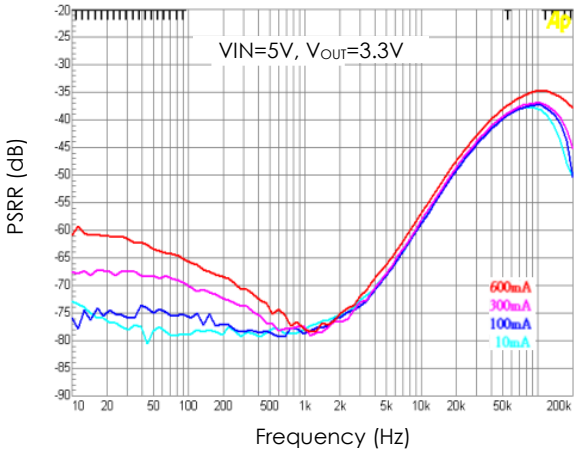
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN.

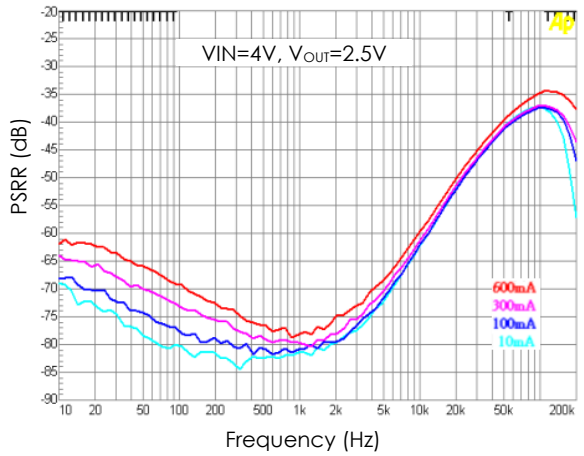
PSRR vs. Frequency



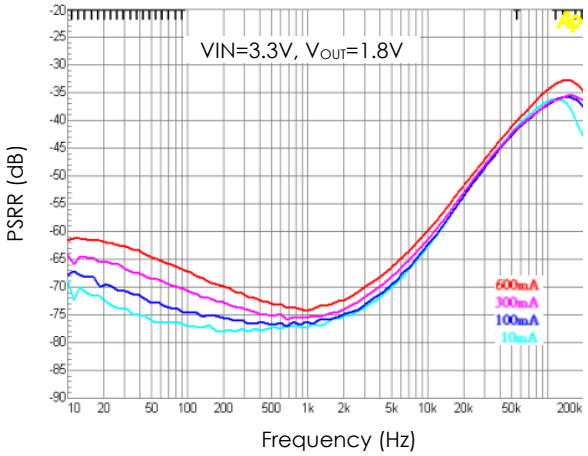
PSRR vs. Frequency



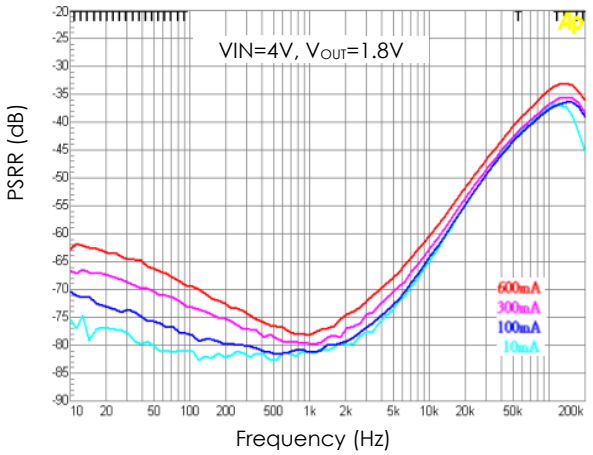
PSRR vs. Frequency



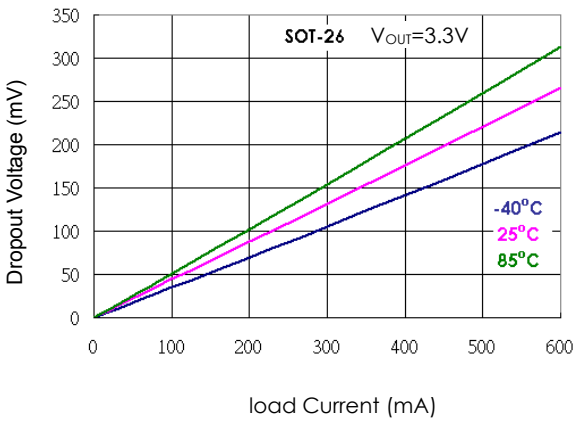
PSRR vs. Frequency



PSRR vs. Frequency



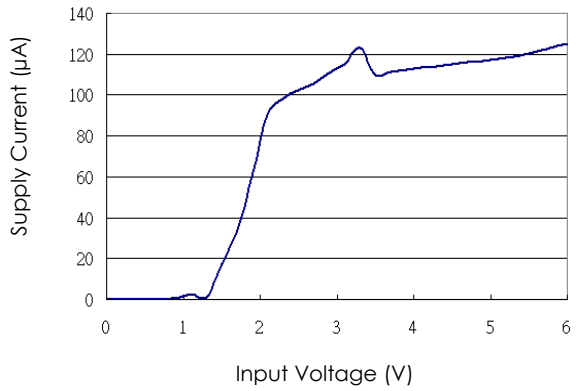
Dropout Voltage vs. Load Current



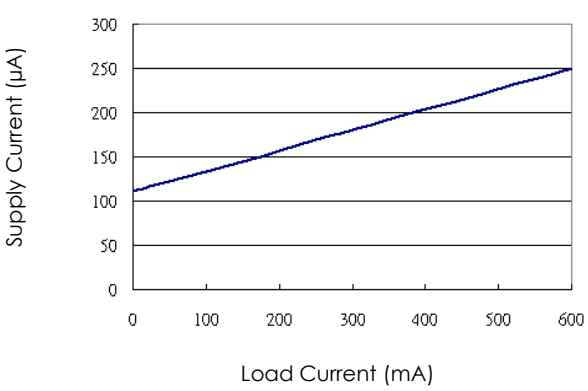
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN. (Continued)

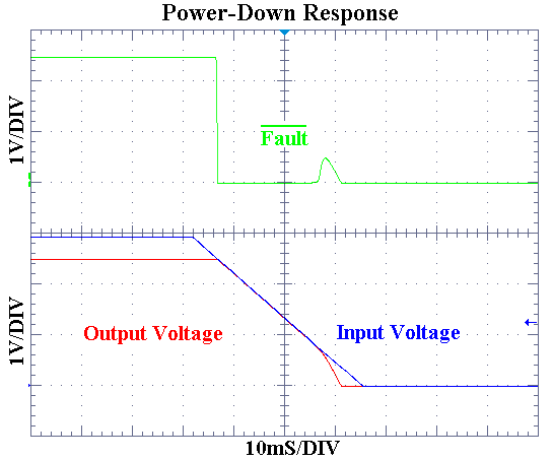
Supply Current vs. Input Voltage



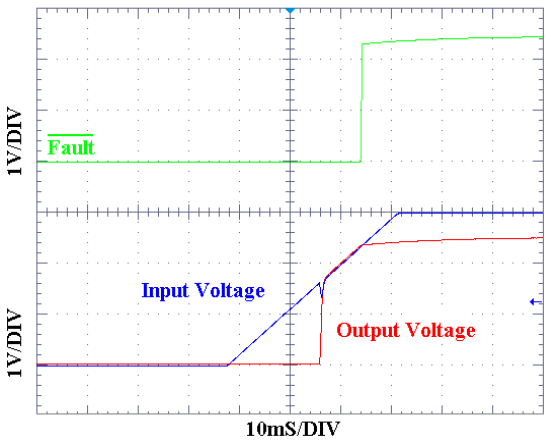
Supply Current vs. Load Current



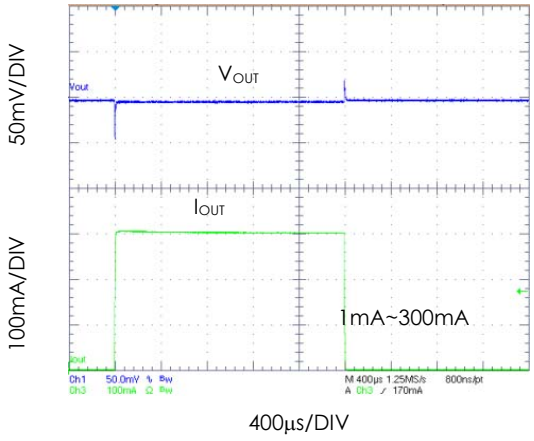
Power-Down Response



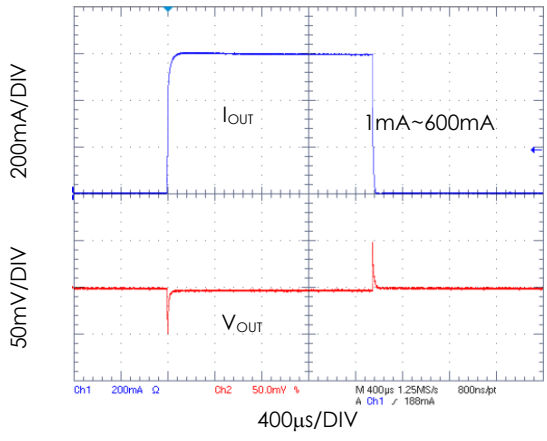
Power-Up Response



Load Transient



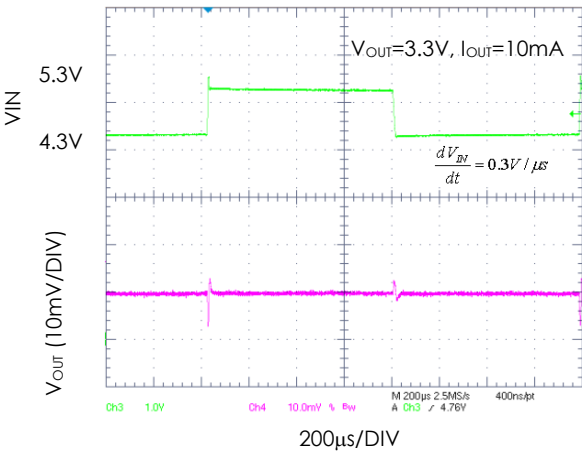
Load Transient



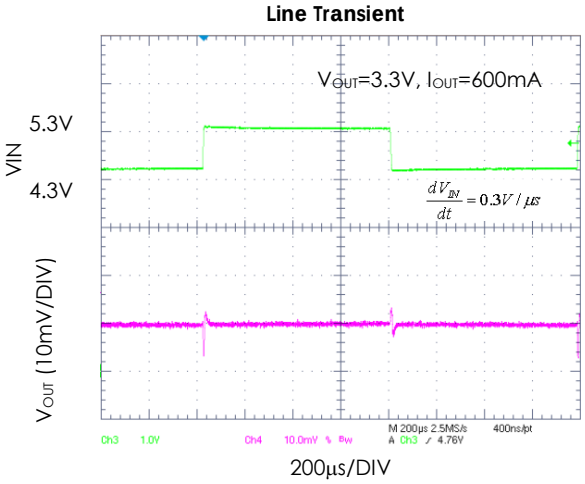
Typical Performance Characteristics

Unless otherwise specified, VIN = $V_{OUT\ (NOM)}$ + 1V, C_{IN} = C_{OUT} = 2.2µF, C_{CC} = 33nF, T_A = 25°C, $V_{\overline{SHDN}}$ = VIN. (Continued)

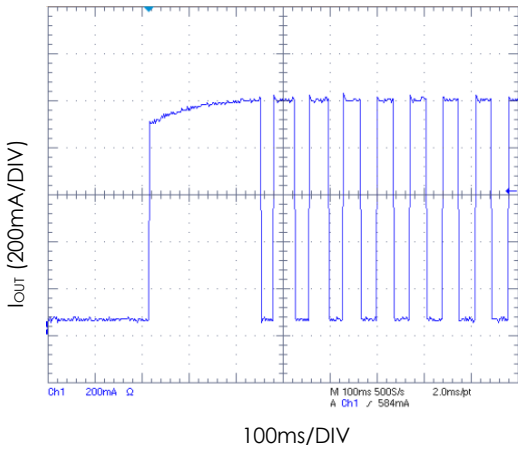
Line Transient



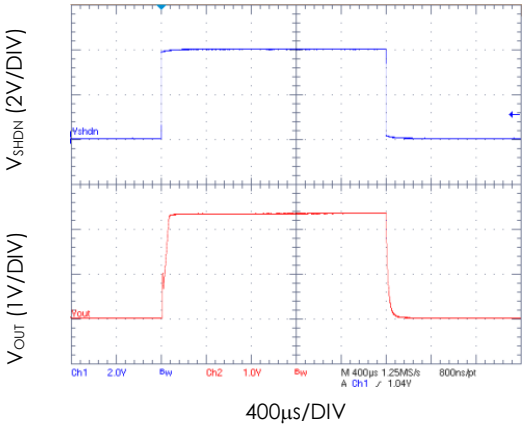
Line Transient



Current Limit



Enable and Disable



Application Information

General Description

Referring to Figure 2 as shown in the Functional Block Diagram section, the EMP8966 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R1, R2) to sample the output voltage for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage. These feedback resistors can be either internal or external to the EMP8966, depending on whether a preset or an adjustable output voltage version is being used.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the fault detection, and the temperature and current protection circuitry.

Output Voltage Control

The EMP8966 allows direct user control of the output voltage in accordance with the amount of negative feedback present. To see the explicit relationship between the output voltage and the negative feedback, it is convenient to conceptualize the EMP8966 as an ideal non-inverting operational amplifier with a fixed DC reference voltage VREF at its non-inverting input. Such a conceptual representation

of the EMP8966 in closed-loop configuration is shown in Figure 3. This ideal op amp features an ultra-high input resistance such that its inverting input voltage is virtually fixed at VREF. The output voltage is therefore given by:

$$V_{OUT} = V_{REF}\left[\frac{R_1}{R_2} + 1\right]$$

This equation can be rewritten in the following form to facilitate the determination of the resistor values for a chosen output voltage:

$$R_1 = R_2\left[\frac{V_{OUT}}{1.19V} - 1\right]$$

Set R2 equal to 100kΩ to optimize for overall accuracy, power supply rejection, noise, and power consumption.

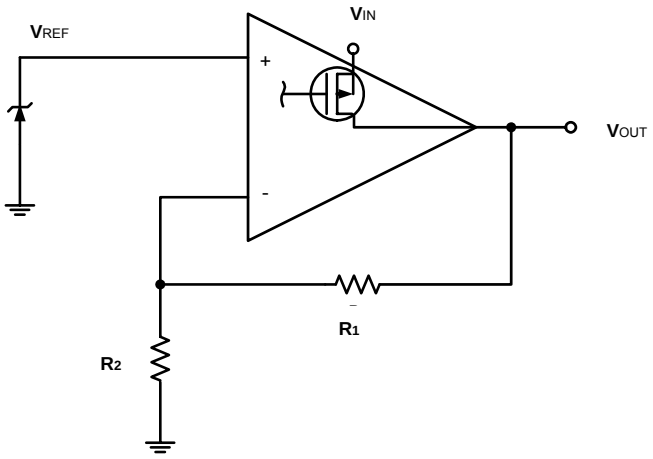


Figure 3. Simplified Regulator Topology

Output Capacitor

The EMP8966 is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the

Application Information (Continued)

battery power source. Typical ceramic capacitors suitable for use with the EMP8966 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8966 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8966 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8966. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the EMP8966 is accomplished through the connection of the noise bypass capacitor CC (33nF optimum) between pin 4(sot-23-6) and the ground. Because pin 4(sot-23-6) connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the CC capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the CC capacitor types for use with the EMP8966. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the CC capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Tradeoff exists between output noise level and turn-on time when selecting the CC capacitor value.

Power Dissipation and Thermal Shutdown

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The EMP8966 relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature TJ exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θJA and TJ is as follows:

$$T_J = \theta_{JA} (PD) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$$P_D = I_{OUT} (V_{IN} - V_{OUT})$$

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8966, refrain from exceeding the absolute maximum junction temperature rating of

Application Information (Continued)

150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly. **Shutdown**

The EMP8966 enters the sleep mode when the $\overline{SHDN}$ pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the EMP8966 best suited for battery-powered applications. The maximum guaranteed voltage at the $\overline{SHDN}$ pin for the sleep mode to take effect is 0.4V. A minimum guaranteed

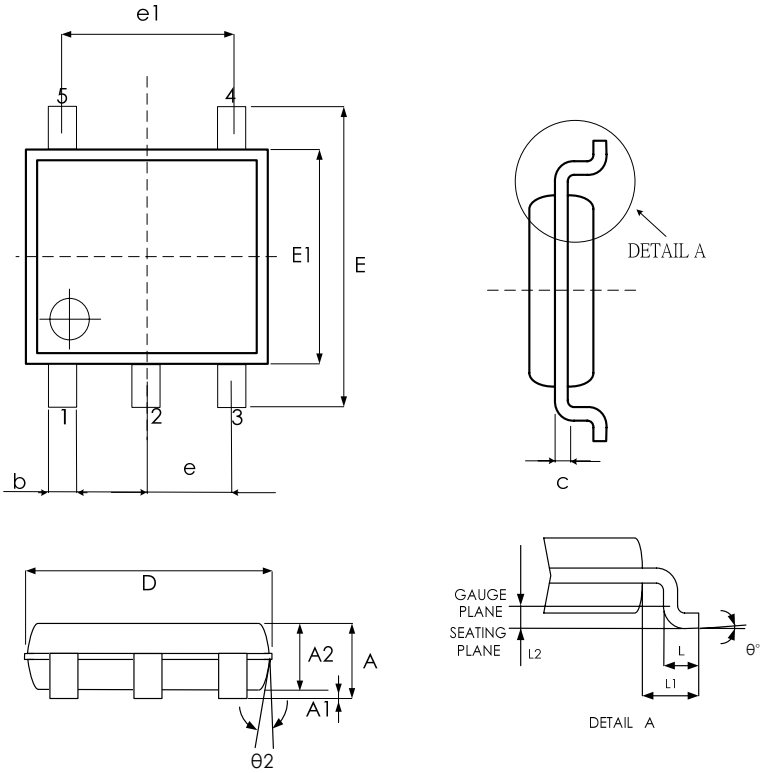
voltage of 1.2V at the $\overline{SHDN}$ pin will activate the EMP8966. Direct connection of the $\overline{SHDN}$ pin to the VIN to keep the regulator on is allowed for the EMP8966. In this case, the $\overline{SHDN}$ pin must not exceed the supply voltage VIN.

Fast Start-Up

Fast start-up time is important for overall system efficiency improvement. The EMP8966 assures fast start-up speed when using the optional noise bypass capacitor (CC). To shorten start-up time, the EMP8966 internally supplies a 500μA current to charge up the capacitor until it reaches about 90% of its final value.

Physical Dimensions

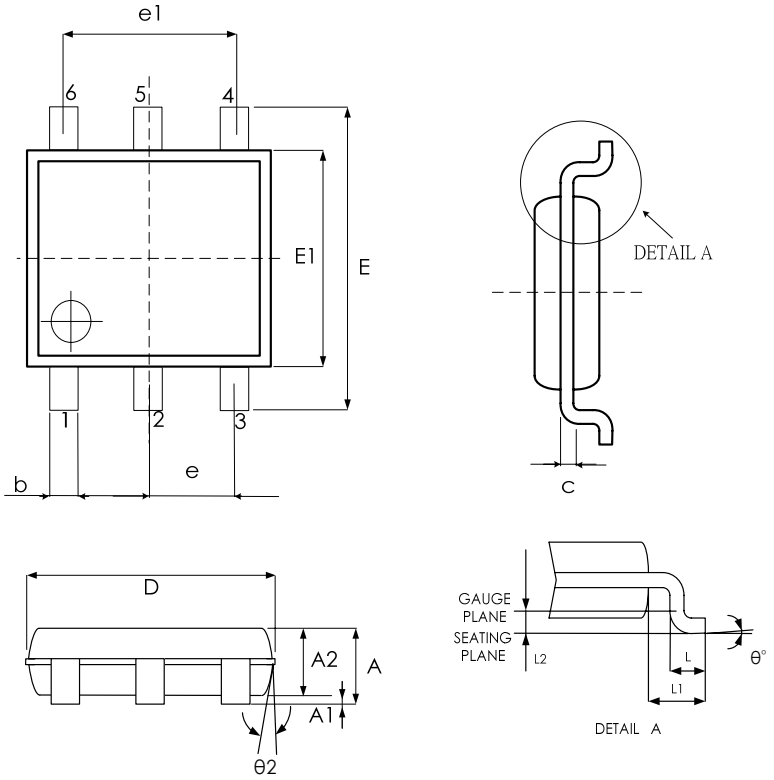
SOT-23-5



SYMBPLS	MIN.	NOM.	MAX.
A	1.05	1.20	1.35
A1	0.05	0.10	0.15
A2	1.00	1.10	1.20
b	0.30	—	0.50
c	0.08	—	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.55
L1	0.60 REF		
θ°	0	5	10
θ2°	6	8	10

UNIT: MM

SOT-23-6



SYMBPLS	MIN.	NOM.	MAX.
A	—	—	1.45
A1	—	—	0.15
A2	0.90	1.15	1.30
b	0.30	—	0.50
c	0.08	—	0.22
D	2.90 BSC.		
E	2.80 BSC.		
E1	1.60 BSC.		
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
L1	0.60 REF		
L2	0.25 REF		
θ°	0	4	8
θ2°	5	10	15

UNIT: MM

Notice

Order, Mark & Packing Information

No. of PIN	Adj	EN	CC	Vout	Package	Old Marking		Product ID
5	Y	Y	N	Adj	SOT-23-5	P630	P630 Date Code	EMP8966-00VF05GRR
						8965 Tracking Code		
6	Y	Y	Y	Adj	SOT-23-6	P630	P630 Date Code	EMP8966-00VC06GRR

Package & Packing

SOT-23-5	3K units Tape & Reel
SOT-23-6	3K units Tape & Reel

Revision History

Revision	Date	Description
1.0	2008.10.07	Original
1.1	2009.05.08	Modify order information
1.2	2014.12.29	Remove SOT-89-5

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express , implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.